

# PATENT ABSTRACTS OF JAPAN

(11)Publication number : 11-284126

(43)Date of publication of application : 15.10.1999

(51)Int.Cl.

H01L 25/16

(21)Application number : 10-087457

(71)Applicant : OTSUKA KANJI  
FUJITSU LTD  
OKI ELECTRIC IND CO LTD  
SANYO ELECTRIC CO LTD  
SHARP CORP  
SONY CORP  
TOSHIBA CORP  
NEC CORP  
HITACHI LTD  
MATSUSHITA ELECTRON CORP  
MITSUBISHI ELECTRIC CORP

(22)Date of filing : 31.03.1998

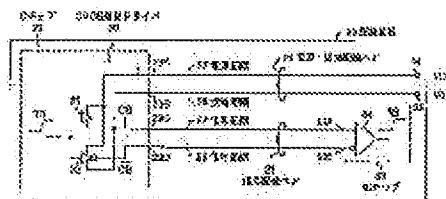
(72)Inventor : OTSUKA KANJI

## (54) ELECTRONIC DEVICE

### (57)Abstract:

PROBLEM TO BE SOLVED: To supply to a differential driver at a high speed without damping complementary signal energy and contrive to increase a speed in transmission of a complementary transmission digital signal to be output by a method wherein first and second power supply wirings for supplying first and second power supply voltages to the differential driver are set as an iso-length parallel wiring.

SOLUTION: A signal wiring pair 21 comprising an iso-length parallel power supply wiring 27 having a large coupling coefficient, a power supply and ground wiring pair 26 comprising a ground wiring 28, and iso-length parallel signal wirings 22, 23 having a large coupling coefficient is provided on a wiring substrate 20. Here, characteristic impedances of the power supply and ground wiring pair 26 and the signal wiring pair are equalized. And, on-resistance of a CMOS differential driver 30 is matched to the characteristic impedance of the signal wiring pair 21 to absorb a reflection complementary transmission digital signal CS./CS reversely transmitted in the signal wiring pair 21. Thus, a waveforms deformation is eliminated, and the complementary transmission digital signal CS./CS can be transmitted at a speed near to a speed of lights.



## LEGAL STATUS

[Date of request for examination] 28.12.2000

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number] 3480306

[Date of registration] 10.10.2003

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

(19) 日本国特許庁 (J P)

(12) 公開特許公報 (A)

(11) 特許出願公開番号

特開平11-284126

(43) 公開日 平成11年(1999)10月15日

(51) Int.Cl.<sup>6</sup>  
H 0 1 L 25/16

識別記号

F 1  
H 0 1 L 25/16

Z

審査請求 未請求 請求項の数24 O L (全 44 頁)

(21) 出願番号 特願平10-87457

(22) 出願日 平成10年(1998) 3 月31日

(71) 出願人 598042633

大塚 寛治

東京都東大和市御幸 2 -1074-38

(71) 出願人 000005223

富士通株式会社

神奈川県川崎市中原区上小田中4丁目1番  
1号

(71) 出願人 000000295

沖電気工業株式会社

東京都港区虎ノ門1丁目7番12号

(74) 代理人 弁理士 平戸 哲夫

最終頁に続く

(54) 【発明の名称】 電子装置

(57) 【要約】

【課題】 ドライバから出力される送信デジタル信号を信号配線を介してレシーバに伝送する伝送回路を有する電子装置に関し、信号伝送の高速化を図る。

【解決手段】 配線基板 20 に形成する電源配線 27 及び接地配線 28 をカップリング係数を大とする等長平行配線からなるペア配線構造とし、CMOS 差動ドライバ 30 に供給すべき相補信号エネルギーに対して電源・接地配線ペア 26 を電磁界がほぼ閉じた伝送線路として機能させる。

本発明の第 1 実施形態の構成図

